IN THE CLAIMS:

Cancel claims 7, 8, 25, and 26. Please amend claims 1, 3, 9, 10, 19, 21, 27, and 28 as set forth in Appendix A attached hereto. Applicant notes that all claims currently pending in the application are shown below, in the proposed amended form, for clarity, except claims 7, 8, 25, and 26 which are canceled herein.

Dub D1 C1

1. (Three Times Amended) A contact for a semiconductor device, comprising:

a single contact plug extending through a first barrier layer, said single contact plug in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop said single contact plug, wherein said contact land is wider than said single contact plug and is substantially planar;

an upper contact extending through a second barrier layer, said second barrier layer disposed over said first barrier layer to form an electrical contact with said individual contact land.

Dub D2 C2

3. (Three Times Amended) A transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one drain region and said at least one source region on said at least one active area;

a first barrier layer substantially covering said at least one field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one source region on said semiconductor substrate;

an individual drain contact land disposed atop each of said at least one drain contact plugs, said individual drain contact land wider than said at least one drain contact plug and substantially planar;

an individual source contact land disposed atop each of said at least one source contact plugs, said individual source contact land wider than said at least one source contact plug and substantially planar;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, said at least one upper source contact is in electrical communication with at least one of said individual source contact lands; and

at least one upper drain contact extending through said second barrier layer, said at least one upper drain contact in electrical communication with at least one of said individual drain contact lands.

4. (Amended) The transistor of claim 3, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

5. (Twice Amended) The transistor of claim 3, wherein said at least one source contact plug extends between at least two source regions.

6. (Twice Amended) The transistor of claim 3, wherein said at least one drain contact plug extends between at least two drain regions.

7. (Canceled)

8. (Canceled)

9. (Three Times Amended) The transistor of claim 3, wherein said at least one upper source contact extends between at least two individual source contact lands.

10. (Three Times Amended) The transistor of claim 3, wherein said at least one upper drain contact extends between at least two individual drain contact lands.

19. (Twice Amended) A semiconductor device including at least one contact, comprising:

a single contact plug extending through a first barrier layer, said single contact plug in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop said single contact plug, said individual contact land wider than said single contact plug and substantially planar; and

an upper contact extending through a second barrier layer, said second barrier layer disposed over said first barrier layer to form an electrical contact with said individual contact land.

21. (Three Times Amended) A semiconductor device including at least one transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer substantially covering said at least one thick field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one implanted drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one implanted source region on said semiconductor substrate;

an individual drain contact land disposed atop said at least one drain contact plug, said individual drain contact land wider than said at least one drain contact plug;

an individual source contact land disposed atop said at least one source contact plug, said individual source contact land is wider than said at least one source contact plug;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, said at least one upper source contact in electrical communication with at least one said individual source contact land; and

at least one upper drain contact extending through said second barrier layer, said at least one upper drain contact in electrical communication with at least one said individual drain contact land.

22. The semiconductor device of claim 21, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

23. (Amended) The semiconductor device of claim 21, wherein said at least one source contact plug extends between at least two source regions.

24. (Amended) The semiconductor device of claim 21, wherein said at least one drain contact plug extends between at least two drain regions.

25. (Canceled)

26. (Canceled)

27. (Amended) The semiconductor device of claim 21, wherein said at least one upper source contact extends between at least two individual source contact lands.

28. (Twice Amended) The semiconductor device of claim 21, wherein said at least one upper drain contact extends between at least two individual drain contact lands.